

**Amendments to the Specification:**

Please replace the paragraph [0039] with the following corrected paragraph:

--Overlying insulator layer 27 is disposed over doped regions 28, 30a, 32a, and gate electrode 35. Insulator layer 27 may be formed of deposited silicon dioxide, another deposited inorganic insulator, or a spin-on type organic or inorganic layer, depending upon the particular manufacturing processes used. Contact openings C are etched through insulator layer 27 in the conventional manner, followed by the deposition and patterned etching of a metal conductor layer, to form metal conductors BG, S, and D which make contact to doped regions 28, 30a, 32a of transistor 40 as shown. As shown in Figure 3c, contact openings C are also etched through insulator layer 27, so that contact can be made to gate electrode ~~35~~ 45 by a metal conductor (metal not being shown in Figure 3c). As known in the art, additional levels of metal conductors may be formed, and indeed various ones of the conductors making contact to the elements of transistor 40 may be formed in different metal layers, depending upon the layout of the integrated circuit.--